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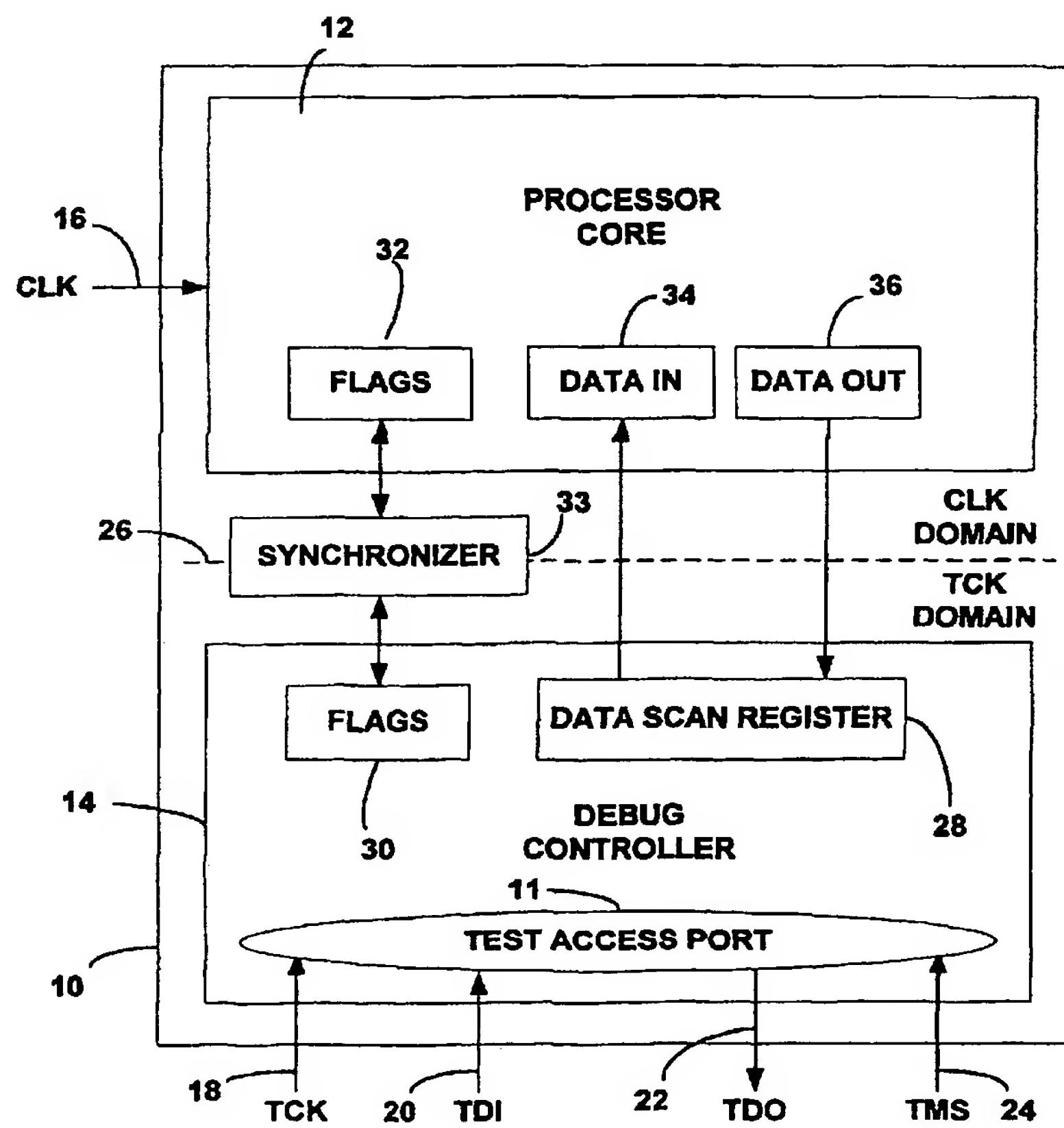
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(54) Title: DATA SYNCHRONIZATION FOR A TEST ACCESS PORT



(57) Abstract: In one embodiment, an integrated circuit provides a test access port that communicates with scan chain registers in a processor core. The integrated circuit synchronizes data transferred between a debug controller that operates under control of a test clock (TCK) and the processor core that operates under control of a processor clock (CLK).

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